WHAT IS CLAIMED IS:

1. In a logic inverter; comprising an n-channel and a p-channel field-effect transistor, and a polysilicon gate extending over their respective channels, the improvement comprising:

a) a polysilicon conductor connecting drains of the two transistors.

2. Apparatus according to claim 1 in which the polysilicon conductor and the polysilicon gate are substantially coplanar.

3. In an integrated circuit which includes multiple layers of interconnect, the improvement comprising:

a) a layer of interconnect comprising local interconnect, and containing no non-local interconnect.

4. In an integrated circuit which includes multiple layers of interconnect, the improvement comprising:

a) different spacings between adjacent interconnect traces on one of the layers.

5. In a method of constructing a logic inverter which comprises an n-channel and a p-channel field-effect transistor, the improvement comprising:

a) etching

i) a gate electrode and

ii) a conductor connecting drains of the two transistors from a single layer of polysilicon.

6. An integrated circuit, comprising:

a) a standard cell array comprising rows of cells having a row pitch; and

b) a MACRO, embedded within the standard cell array, comprising rows of cells having pitch substantially equal to the row pitch.

7. An integrated circuit, comprising:

a) a standard cell array region, comprising rows of cells having a ROW PITCH;

b) a pair of power conductors extending across each row; and

c) a MACRO region, comprising rows of cells having a pitch equal to said row pitch.

8. An integrated circuit, comprising:

a) cells of a standard cell array;

b) cells of a MACRO, which have different characteristics from those of the standard cell array and

c) parallel power conductors running adjacent all of said cells.

9. An integrated circuit, comprising:

a) a MACRO embedded in a standard cell array, having substantially the same row pitch as that of the standard cell array;

b) parallel power busses which supply both the MACRO and the standard cell array;

c) a level of metallization which is free of local interconnect;

d) in said level of metallization, interconnect traces having non-uniform spacing; and

e) CMOS inverters, utilized by the IC, in which drain-drain interconnect is constructed from polysilicon.

10. Apparatus according to claim 1 and further comprising a layer of interconnect traces which contains exclusively global interconnect.

11. Apparatus according to claim 10 in which the layer of interconnect traces have a non-uniform spacing.

12. Apparatus according to claim 1 and further comprising:

b) a standard cell array comprising rows of cells having a row pitch;

c) a MACRO, embedded within the standard cell array, comprising rows of cells having pitch substantially equal to the row pitch.

13. A method of constructing an integrated circuit, comprising the following steps:

a) running multiple computer simulations of a MACRO which is

i) embedded in a standard cell array; and

ii) constructed of transistors contained within the array;

b) changing dimensions of transistors in different simulations;

c) identifying transistor dimensions which provide superior timing performance; and

d) fabricating the embedded MACRO according to the identified dimensions of paragraph (c).